

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. 1875.2800001	APPLICATION NO. To Be Assigned 10/720144
	APPLICANT Mulder et al.	
	FILING DATE Herewith 11/25/03	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
RL	AA1	6,259,745 B1	07/2001	Chan	375	285	
RL	AB1	5,554,943	09/1996	Moreland	327	65	
RL	AC1	5,118,971	06/1992	Schenck	326	32	
RL	AD1	5,006,727	04/1991	Ragosch et al.	327	65	
RL	AE1	4,959,563	09/1990	Schenck	326	32	
ATL	AF1	3,846,712	11/1974	Kiko	330	30	
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
RL	AR	1	Abo, A.M. and Gray, P.R., "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 5, May 1999, pp. 599-606.
RL	AS	1	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1788-1795.
RL	AT	1	Bult, Klaas and Buchwald, Aaron, "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1- μ m," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 32, No. 12, December 1997, pp. 1887-1895.

EXAMINER LULU	DATE CONSIDERED 5/27/04
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2						
	AB2						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
AK	AR	2	Cho, T.B. and Gray, P.R., "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 3, March 1995, pp. 166-172.
AK	AS	2	Choe, M-J. et al., "A 13-b 40-Msamples/s CMOS Pipelined Folding ADC with Background Offset Trimming," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pp. 1781-1790.
AK	AT	2	Choi, M. and Abidi, A., "A 6-b 1.3-Gsample/s A/D Converter in 0.35- μ m CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 12, December 2001, pp. 1847-1858.

EXAMINER	DATE CONSIDERED
LLM	5/27/04

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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3						
	AB3						
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	AK3						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

ALC	AR	3	Flynn, M. and Sheahan, B., "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 33, No. 12, December 1998, pp. 1932-1938.
ALC	AS	3	Geelen, G., "A 6b 1.1GSample/s CMOS A/D Converter," <i>IEEE International Solid-State Circuits Conference</i> , IEEE, 2001, pp. 128-129 and 438.
ALC	AT	3	Hoogzaad, G. and Roovers, R., "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 μm^2 ," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1796-1802.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA4						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
AC	AR	4	Hosotani, S. et al., "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW Power Consumption," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 25, No. 1, February 1990, pp. 167-172.
AC	AS	4	Ingino, J.M. and Wooley, B.A., "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 33, No. 12, December 1998, pp. 1920-1931.
AC	AT	4	Ito, M. et al., "A 10 bit 20 MS/s 3 V Supply CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 29, No. 12, December 1994, pp. 1531-1536.

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	AA5						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL5						Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AA	AR	5	Kattman, K. and Barrow, J., "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters," <i>IEEE International Solid-State Conference</i> , IEEE, 1991, pp. 170-171.
AC	AS	5	Kusumoto, K. et al., "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 28, No. 12, December 1993, pp. 1200-1206.
AL	AT	5	Lewis, S. et al., "A 10-b 20-Msample/s Analog-to-Digital Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 27, No. 3, March 1992, pp. 351-358.

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	APPLICANT Mulder et al.	
	FILING DATE Herewith 11/25/03	GROUP To Be Assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA6						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
AK	AR	6	Mehr, I. and Singer, L., "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 3, March 2000, pp. 318-325.
AK	AS	6	Nagaraj, K. et al., "Efficient 6-Bit A/D Converter Using a 1-Bit Folding Front End," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 8, August 1999, pp. 1056-1062.
AK	AT	6	Nagaraj, K. et al., "A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25- μ m Digital CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pp. 1760-1768.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL7						Yes No
	AM7						Yes No
	AN7						Yes No
	AO7						Yes No
	AP7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

<u>ALU</u>	AR	2	Nauta, B. and Venes, A., "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 12, December 1995, pp. 1302-1308.
<u>ALU</u>	AS	2	Pan, H. et al., "A 3.3-V 12-b 50-MS/s A/D Converter in 0.6- μ m CMOS with over 80-dB SFDR," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pp. 1769-1780.
<u>ALU</u>	AT	2	Song, W-C. et al., "A 10-b 20-Msample/s Low-Power CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 5, May 1995, pp. 514-521.

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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL8						Yes No
	AM8						Yes No
	AN8						Yes No
	AO8						Yes No
	AP8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
ku	AR	8	Sumanen, L. et al., "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 7, July 2001, pp. 1048-1055.
aa	AS	8	Taft, R.C. and Tursi, M.R., "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 3, March 2001, pp. 331-338.
ku	AT	8	van der Ploeg, H. and Remmers, R., "A 3.3-V, 10-b 25-Msample/s Two-Step ADC in 0.35- μ m CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pp. 1803-1811.

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.2800001	APPLICATION NO. To Be Assigned 10/720/44
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
	AB9						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL9						Yes No
	AM9						Yes No
	AN9						Yes No
	AO9						Yes No
	AP9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
HL	AR	2	van der Ploeg, H. et al., "A 2.5-V 12-b 54-Msample/s 0.25- μ m CMOS ADC in 1-mm ² With Mixed-Signal Chopping and Calibration," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 12, December 2001, pp. 1859-1867.
HL	AS	2	Vorenkamp, P. and Roovers, R., "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 32, No. 12, December 1997, pp. 1876-1886.
HL	AT	2	Wang, Y-T. and Razavi, B., "An 8-bit 150-MHz CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 3, March 2000, pp. 308-317.

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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10						
	AB10						
	AC10						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL10						Yes No
	AM10						Yes No
	AN10						Yes No
	AO10						Yes No
	AP10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
AK	AR	10	Yotsuyanagi, M. et al., "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 12, December 1995, pp. 1533-1537.
KU	AS	10	Yu, P.C. and Lee, H-S., "A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 31, No. 12, December 1996, pp. 1854-1861.
KU	AT	10	Miyazaki et al., "A 16mW 30MSample/s 10b Pipelined A/D Converter using a Pseudo-Differential Architecture", <i>ISSCC 2002/Session 10/High-Speed ADCs/10.5</i> , February 5, 2002, 3 pgs.

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.2800001/RES/GSB	APPLICATION NO. To Be Assigned 10/720/44
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA11						
	AB11						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL11						Yes No
	AM11						Yes No
	AN11						Yes No
	AO11						Yes No
	AP11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
tu	AR	11	Sushihara et al., "A 7b 450MSample/s 50mW CMOS ADC in 0.3 mm ² ", ISSCC 2002/Session 10/High-Speed ADCs/10.3, February 5, 2002, 3 pgs.
tu	AS	11	Dingwall et al., "An 8-MHz CMOS Subranging 8-Bit A/D Converter", IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 6, December 1985, pp. 1138-1143.
	AT	11	

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